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AMENDMENTS TO THE CLAIMS:

1. (Currently amended): A thin film transistor on a substrate comprising:

a semiconductor layer having a first doped region and a second doped region in between a first further doped region and a second further doped region, and having an undoped region in between the first doped region and the second doped region, the first doped region and the second doped region having a lower conductivity than the first further doped region and the second further doped region; and

an oxide layer partially covering a surface of the semiconductor layer, the oxide layer carrying:

[[-]] a conductive gate over the undoped region having a first side and a second side substantially perpendicular to the oxide layer;

[[-]] a first conductive spacer and a second conductive spacer adjacent to the first side and second side of the conductive gate respectively;

[[-]] a first insulating spacer adjacent to a side of the first conductive spacer opposite the first side of the conductive gate; and

[[-]] a second insulating spacer adjacent to a side of the second conductive spacer opposite the second side of the conductive gate;

the thin film transistor further comprising:

a first conductive contact with the first further doped region; and

a second conductive contact with the second further doped region.

2. (Canceled)

3. (Previously presented): A thin film transistor as claimed in claim 1, wherein the first conductive contact and the second conductive contact comprise a silicide layer.

4. (Previously presented): A thin film transistor as claimed in claim 1, wherein the semiconductor layer comprises a polycrystalline silicon material.

5-8. (Canceled)

9. (Currently amended): An electronic device comprising an active matrix array coupled to a first driver circuit arrangement and a second driver circuit arrangement, the first driver circuit arrangement and the second driver circuit arrangement being coupled to a power supply, at least one of the active matrix array, the first driver circuit arrangement and the second driver circuit arrangement comprising a plurality of thin film transistors as claimed in claim 1 ~~any of the claims 1-4~~.

10. (Previously presented): An electronic device as claimed in claim 9, wherein the power supply comprises battery means.

11-13. (Canceled)

14. (New): An active matrix array, comprising a plurality of matrix elements, each comprising a thin film transistor as claimed in claim 1.

15. (New): A thin film transistor, comprising:

a substrate;

a semiconductor layer supported on the substrate, including an undoped region, a first doped region and a second doped region, and a first further doped region and a second further doped region, wherein the first doped region is between the undoped region and the first further doped region, and the second doped region is between the undoped region and the first further doped region;

a gate supported above the semiconductor layer;

a first insulating spacer disposed at a first side of the gate and a second insulating spacer disposed at a second side of the gate; and

a first conductive spacer between the first insulating spacer and the gate, and a second conductive spacer between the second insulating spacer and the gate.

16. (New): A thin film transistor as claimed in claim 15, wherein the first conductive spacer is directly above the first doped region and the second conductive spacer is directly above the second doped region.

17. (New): A thin film transistor as claimed in claim 16, wherein the first side of the gate is aligned with a first edge of the undoped region, and the second side of the gate is aligned with a second edge of the undoped region.

18. (New): A thin film transistor as claimed in claim 17, wherein a first edge of the first conductive spacer away from the gate is aligned with a first edge of the first doped region away

from the undoped region, and a second edge of the second conductive spacer away from the gate is aligned with a second edge of the second doped region away from the undoped region.

19. (New): A thin film transistor as claimed in claim 18, further comprising:

an oxide layer covering the undoped region, the first doped region and the second doped region, and partially covering the first further doped region and the second further doped region, wherein the oxide layer supports the gate, the first conductive spacer, the second conductive spacer, the first insulating spacer, and the second insulating spacer.

20. (New): A thin film transistor as claimed in claim 19, wherein a first edge of the first insulating spacer away from the first conductive spacer is aligned with a first edge of the oxide layer, and a second edge of the second insulating spacer away from the second conductive spacer is aligned with a second edge of the oxide layer.

21. (New): A thin film transistor as claimed in claim 20, further comprising:

a first conductive contact with the first further doped region; and

a second conductive contact with the second further doped region.

22. (New): A thin film transistor as claimed in claim 15, wherein the first conductive spacer is adjoining a first side of the gate, and the second conductive spacer is adjoining a second side of the gate.

23. (New): A thin film transistor as claimed in claim 15, wherein the first insulating spacer is adjoining the first conductive spacer away from the gate, and the second insulating

spacer is adjoining the second conductive spacer away from the gate.

24 (New): An active matrix array, comprising a plurality of matrix elements, each including a thin film transistor as in claim 15.

25. (New): An electronic device, comprising:

an active matrix array as in claim 24; and

at least one driver circuit operatively coupled to the active matrix array.

26. (New): A method for producing a thin film transistor as in claim 15.